REMARKS

This Amendment responds to the Office Action dated August 25, 2004 in which the Examiner rejected claim 13 under 35 U.S.C. § 112, second paragraph and rejected claims 12-15 under 35 U.S.C. § 103.

As indicated above, a minor informality in claim 13 has been corrected. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claim 13 under 35 U.S.C. § 112, second paragraph.

Claim 12 claims a method for manufacturing an electronic equipment by mounting a semiconductor device on a mounting board with projecting electrodes interposed therebetween. The semiconductor device has the projecting electrodes and a semiconductor chip both provided on a mounting side thereof, and has an electronic component provided on a side opposite to the mounting side. The semiconductor chip has a thickness smaller than a height of the projecting electrodes. The electronic component has a thickness larger than that of the semiconductor chip. The semiconductor device is mounted on the mounting board with the projecting electrodes interposed therebetween by aligning with the mounting board the semiconductor device, which is warped so as to be recessed on the mounting side, and pressing the semiconductor device on the mounting board with the semiconductor device being in the warped state.

Through the method of the claimed invention having a semiconductor device which has a semiconductor chip provided on a mounting side and being warped to be recessed on the mounting side, as claimed in claim 12, the claimed invention provides a method of manufacturing an electronic equipment in which the semiconductor chip will not contact the mounting board when the semiconductor

device is mounted on a mounting board. The prior art does not show, teach or suggest the invention as claimed in claim 12.

Claims 12 and 13 were rejected under 35 U.S.C. § 103 as being unpatentable over *Degani et al.* (U.S. Patent No. 6,437,990) in view of *Ishibashi* (Japanese Reference 2000-031316).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

Degani et al. appears to disclose a BGA package designed as shown in FIG. 2, where the IC chip is designated 21 and is die bonded to interconnect substrate 22 as in FIG. 1. Bond pads 23 on the IC chip are interconnected to bond pads 24 on the interconnect substrate by wire bonds 25. The substrate 22 is interconnected to motherboard 26, by solder balls 27 and BGA bond pads 28. Attached to the underside of the substrate 22, in the BGA gap, is an array of IC chips 31-34. Each of the array of IC chips is flip-chip bonded to the underside of substrate 22 using solder bumps 35. Solder bumps 35 are typically provided with under bump metallization (not shown). Substrate 22 therefore supports a hybrid of wire bonded chips and solder bonded flip-chips. In the preferred embodiment of the invention the wire bonded IC chip 21 is a logic/controller IC chip and the IC chips 31-34 in the array on the underside of substrate 22 are memory IC chips. (col. 2, lines 48-64)

Thus, *Degani et al.* merely discloses a IC chip 21 mounted on an interconnection substrate 22 on a first surface while IC chips 31-34 are mounted on a second surface of the interconnect substrate 22. Nothing in *Degani et al.* shows,

teaches or suggests a semiconductor device warped to be recessed on a mounting side where a semiconductor chip having a small thickness is mounted as claimed in claim 12. Rather, *Degani et al.* merely discloses mounting IC chips 21, 31-34 mounted on different surfaces of an interconnect board 22 (i.e. *Degani et al.* is silent about warping to be recessed).

Ishibashi appears to disclose to stably mount a semiconductor device on a mother board through solder balls at a low cost regardless of the warping state of the device by providing a surface mount jig which supports the semiconductor device separately from a mother board at the time of reflowing the solder balls between the mother board and semiconductor device. A surface mount jig 1 which is used for supporting an intermediate board 3 is provided on a mother board 4 having board pads 8 and solder balls 2 are formed on the rear surface of the intermediate board 3 to which a semiconductor chip 6 is bonded with a mount material 7. At the time of bonding the intermediate board 3 to the mother board 4, solder balls are sufficiently melted by prolonging the reflow heating time or raising the temperature. At the time of bonding the board 3 to the board 4, in addition, the occurrence of such a state that the solder balls 2 are crushed and protrude from the board pads 8 is avoided by supporting the board 3 by the surface mount jig 1 from four sides. Therefore, the intermediate board 3 can be easily arranged on a prescribed position of the mother board 4 by means of the jig 1.

Thus, *Ishibashi* merely discloses requiring a flat wiring board in order to connect solder balls on a back surface and providing a surface mount jig on a mounting board. Nothing in *Ishibashi* shows, teaches or suggests a semiconductor device is warped to be recessed (with the constituent materials of the semiconductor

device) as claimed in claim 10 (i.e. no surface mounting jig is used in the claimed invention).

Also, *Ishibashi* merely discloses bonding an intermediate board 3 to a mother board 4 using a surface mount jig 1. Nothing in *Ishibashi* shows, teaches or suggests a) a semiconductor device having a semiconductor chip provided on a mounting side, or b) the semiconductor device is warped to be recessed on a mounting side where a semiconductor chip of small thickness is mounted as claimed in claim 12. Rather, *Ishibashi* merely discloses a semiconductor chip 6 mounted on a side opposite to a mounting side while the intermediate board is mounted on a surface mount jig 1.

The combination *Degani et al.* and *Ishibashi* is not possible since *Degani et al.* is silent about warping to be recessed while *Ishibashi* uses a surface mounting jig. Even assuming the references can be combined, the combination of *Degani et al.* and *Ishibashi* would merely suggest that if the substrate 22 of *Degani et al.* is warped, to not use the chips 31-34 as taught by *Ishibashi* and to provide a jig 1 as taught by *Ishibashi*. Therefore, nothing in the combination of *Degani et al.* and *Ishibashi* shows, teaches or suggests a semiconductor device warped to be recessed on a mounting side where a semiconductor chip having a small thickness is mounted as claimed in claim 12. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claim 12 under 35 U.S.C. § 103.

Claim 15 depends from claim 12 and recites the additional feature of bonding an electronic component to a wiring substrate with heating and then cooling such that the wiring substrate is warped and then mounting the semiconductor chip on the mounting side of the wiring substrate. Nothing in *Degani* or *Ishibashi* shows,

teaches or suggests this feature. Therefore, Applicants respectfully submit that claim 15 would not have been obvious within the meaning of 35 U.S.C. § 103 at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claim 15 under 35 U.S.C. § 103.

Claims 13 and 14 were rejected under 35 U.S.C. § 103 as being unpatentable over *Degani et al.* in view of *Ishibashi* and further in view of *Hozoji et al.* (Japanese Reference 10-79405).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, since nothing in the combination of the primary references shows, teaches or suggests the primary features as claimed in claim 12, Applicants respectfully submit that the combination of the primary references with the secondary reference will not overcome the deficiencies of the primary reference. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 13 and 14 under 35 U.S.C. § 103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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